

100-11052  
100-11052

	Class	Subclass	ISSUE CLASSIFICATION
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**PATENT NUMBER**

## **U.S. UTILITY Patent Application**

O.I.P.E.	PATENT DATE
S. I. 	
SCANNED  Q.A. 	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/976052	F	327	333	2816	M. Nguva

REMARKS

Level shift circuit and semiconductor integrated circuit

TITLE

## **ISSUING CLASSIFICATION**

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	(Assistant Examiner)				
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____				ISSUE FEE	
	(Primary Examiner)			Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
	(Legal Instruments Examiner)				

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